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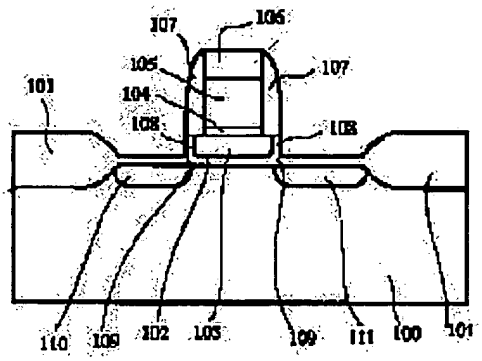
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To decrease the amount of oxide on the surface of tungsten silicide after oxidization, and to suppress the increase of wiring resistance by the forma tion of a silicon nitride film on a tungsten silicide film only.
CONSTITUTION: After a polysilicon film 103 and a high melting point metal silicide film 105 have been formed on a semiconductor substrate 100 through the intermediary of a gate insulating film 102, the first nitride film 106 is formed on the high melting point silicide film 105. The first nitride film 106 and the high melting point metal silicide film 105 are selectively etched, and they are processed into a gate electrode state. Then, the second silicon nitride film 107 is formed on the side wall on the upper part of the gate electrode. Subsequently, the polysilicon film 103 is etched using both silicon nitride films 106 and 107 as a mask, and a lower gate electrode is formed. Subsequently, the side wall of the polysilicon film 103 is rounded by heat-curing (after cure), and a bird's beak 109 is formed between the silicon substrate 100 and the polysilicon film 103.



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CLAIMS

[Claim(s)]
[Claim 1] The manufacture method of a semiconductor device characterized by providing the following. The process which forms a policy contest film through a gate insulator layer on a semiconductor substrate. The process which forms a refractory-metal silicide film on the aforementioned polysilicon contest film. The process which forms the 1st nitride on the aforementioned refractory-metal silicide film. The process which etches alternatively to the 1st nitride of the above, and the aforementioned refractory-metal silicide film, and processes a gate electrode configuration, The process which forms the 2nd nitride in the side attachment wall of the 1st nitride of the above and the aforementioned high-melting point silicide film which were processed into the gate electrode configuration, The process which etches to the aforementioned polysilicon contest film by using the 1st nitride of the above, and the 2nd nitride of the above as a mask, and the process which forms a BAZU beak between the aforementioned polysilicon contest film and the aforementioned semiconductor substrate by performing heat treatment.
[Claim 2] The manufacture method of a semiconductor device characterized by providing the following. The process which forms a policy contest film through a gate insulator layer on a semiconductor substrate. The process which forms the electric conduction film which contains a refractory-metal silicide film further at least through the insulator layer between the gates on the aforementioned polysilicon contest film. The process which forms the 1st nitride on the aforementioned electric conduction film. The process which etches alternatively to the 1st nitride of the above, and the aforementioned electric conduction film, and processes a gate electrode configuration, The process which forms the 2nd nitride in the side attachment wall of the 1st nitride of the above and the aforementioned electric conduction film which were processed into the gate electrode configuration, The process which etches to the aforementioned polysilicon contest film by using the 1st nitride of the above, and the 2nd nitride of the above as a mask, and the process which forms a BAZU beak between the aforementioned polysilicon contest film and the aforementioned semiconductor substrate by performing heat treatment.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the manufacture method of a semiconductor device. Especially, a high-melting point silicide film is used for gate polar-zone material, and it is related with the manufacture method of the ** MOS transistor which performs post-oxidation treatment for improvement in an electrical property.
[0002]
[Description of the Prior Art] Conventionally, in the manufacturing process of an MOS transistor transistor, thermal oxidation of the gate oxide film after processing of the gate electrode called post-oxidization has been performed. After this, in oxidization, the edge of a gate electrode oxidizes and it is roundish. This is called BAZU beak. The electric-field concentration in the gate edge at the time of impressing voltage to the gate is eased by this BAZU beak, and the reliability of the gate oxide film in a gate edge improves by it.
[0003] The cross section of the conventional MOS transistor is shown in [drawing 15], and the manufacture method is shown in order of a process. The LOCOS method (selective oxidation method) is used for the isolation field of P type silicon-substrate 300 front face, and the field oxide film 301 is formed in it. Then, after forming the gate oxide film 302 by thermal oxidation, the polysilicon contest film 303 is deposited and this is processed into a gate electrode configuration. Then, oxidize the polysilicon contest film 303 thermally, while forming the thermal oxidation film 304, it is made roundish at the gate electrode edge, and the BAZU beak 305 is formed between the P type silicon substrate 300 and the polysilicon contest film 303. Then, the source 306 and a drain 307 are formed by diffusing an N type impurity.
[0004] However, when forming an MOS transistor using the process which forms a BAZU beak by post-oxidization and the electric conduction film containing high-melting point silicide films, such as a tungsten silicide film, is used as gate polar-zone material, un-arranging [which is described below] arises. That is, if a thermal oxidation film is formed in a gate electrode front face after processing the gate electrode which consists of a polysilicon contest film (lower layer) and a tungsten silicide film (upper layer), the silicon of the surplus contained in tungsten silicide will be consumed, and oxidization will take place about a tungsten metal. If it oxidizes directly hereafter, without [which does not increase this] forming a natural oxidation film on a polysilicon contest film, and using side attachment walls, such as a nitride, etc. in this state, if it carries out and the bipolar membrane of a polysilicon contest film and a high-melting point silicide film will be used as a gate electrode, silicon will be prevented from moving to the upper tungsten silicide film from a lower layer polysilicon contest film. Consequently, oxidization of a tungsten silicide film will be accelerated. For this reason, the problem that wiring resistance will increase remarkably had arisen. Moreover, if thermal oxidation time is short set up in order to reduce the amount of oxidization of a tungsten silicide film, a BAZU beak will not fully be formed in a gate electrode edge, but the reliability of a gate oxide film will deteriorate.
[0005]
[Problem(s) to be Solved by the Invention] As described above, by the manufacture method of the MOS transistor of the conventional refractory-metal silicide gate, there was a trouble that oxidization of a refractory-metal silicide film will start, consequently wiring resistance will increase by post-oxidization.
[0006] this invention aims at offering the manufacture method of the semiconductor device which forms sufficient BAZU beak collectively about a post-oxidization process, without making wiring resistance increase by removing the above-mentioned fault.
[0007]
[Means for Solving the Problem] The process which forms a policy contest film through a gate insulator layer in this invention on a semiconductor substrate in order to attain the above-mentioned purpose, The process which forms a refractory-metal silicide film on a polysilicon contest film, and the process which forms the 1st nitride on a refractory-metal silicide film, The process which etches alternatively to the 1st nitride and refractory-metal silicide film, and processes a gate electrode configuration, The process which forms the 2nd nitride in the side attachment wall f the 1st nitride and high-melting point silicide film which were processed into the gate electrode configuration, The manufacture method of the semiconductor device characterized by providing the process which etches to a polysilicon c ntest film by using the 1st nitride and the 2nd nitride as a mask, and the process which forms a BAZU beak between a polysilicon contest film and a semiconductor substrate by performing heat treatment is offered.

[0008]
[Function] If a means to provide by this invention is used, since the periphery, i.e., the upper part, and the side-attachment-wall section of a high-melting point silicide film (gate electrode upper part) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (gate electrode lower part) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.
[0009]
[Example] Each example of this invention is explained with reference to a drawing. [Drawing 1] - [drawing 7] is the cross section having shown the 1st example of this invention in order of the process. With reference to a drawing, a manufacturing process is explained in order of below.
[0010] As shown in [drawing 1], the LOCOS method (selective oxidation method) is used for the isolation field on the single-crystal-silicon substrate 100 of P type, and the oxide film 101 for isolation with a thickness of 1 micrometer is formed in it. Then, the gate oxide film 102 with a thickness of 10nm is formed in the field in which the oxide film 101 for isolation on the single-crystal-silicon substrate 100 is not formed by thermal oxidation.
[0011] Then, as shown in [drawing 2], the polysilicon contest film 103 with a thickness of 100nm is formed using the LPCVD method (reduced pressure modified chemical vapor deposition), and Lynn is introduced about [one to 5x1015cm -] two after that using ion-implantation to the polysilicon contest film 103. Then, a film composition ratio (mole ratio) deposits 200nm of tungsten silicide films 105 which are W(tungsten):Si(silicon) =1:2.5-3.0 with DC magnetron-sputtering technology. Then, 100nm of 1st silicon nitride 106 is deposited using the LPCVD method. At this time, the natural oxidation film 104 will exist between the polysilicon contest film 103 and the tungsten silicide film 105.
[0012] Then, the resist which is not illustrated is formed on the silicon nitride 106, and the resist pattern of 0.3-micrometer width of face is formed by using lithography technology. Etching processing is given as it is shown in [drawing 3], using this resist pattern as a mask. That is, the RIE (using reactive ion etching) silicon nitride 106 and the tungsten silicide film 105 are processed into a gate electrode configuration, and a resist is removed. At this time, etching removal of the natural oxidation film 104 is carried out simultaneously. Thus, the upper part of a gate electrode was formed.
[0013] Then, the LPCVD method is used for the whole surface, the 2nd silicon nitride 107 of 100nm thickness is deposited on it, and 100nm etchback of this 2nd silicon nitride 107 is carried out using RIE technology. Consequently, as shown in [drawing 4], the 2nd silicon nitride 107 remains in the gate electrode up (tungsten silicide film 105 and 1st silicon nitride 106) side-attachment-wall section.
[0014] Then, as shown in [drawing 5], RIE is given by using the 1st silicon nitride 106 and the 2nd silicon nitride 107 as a mask, and a lower gate electrode is formed by carrying out etching processing of the polysilicon contest film 103.
[0015] Then, heat treatment called post-oxidization is usually performed. By giving such thermal oxidation, as shown in [drawing 6], the side attachment wall of the polysilicon contest film 103 wears a radius of circle 108, and the BAZU beak 109 is formed between a silicon substrate 100 and the polysilicon contest film 103.
[0016] Then, as shown in [drawing 7], the N type source field 110 and the N type drain field 111 are formed with an ion implantation. Then, a layer insulation film, a metal wiring layer, etc. which are not illustrated are formed.
[0017] If the manufacturing process of this invention is used as explained above, since the periphery, i.e., the upper part, and the side-attachment-wall section of a high-melting point silicide film (gate electrode upper part) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (gate electrode lower part) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.
[0018] In addition, usually, if the bipolar membrane of a polysilicon contest film and a high-melting point silicide film is used as a gate electrode, a natural oxidation film will be formed on a polysilicon contest film. In this state, after oxidizing directly, without using side attachment walls, such as a nitride, etc., silicon was prevented from moving to the upper tungsten silicide film from the polysilicon contest film of a lower layer [film / natural oxidation], and oxidization of the tungsten silicide film concerned was accelerated. However, in this example, even if a natural oxidation film is formed and movement of silicon is oppressed, since the up gate electrode is covered by the nitride, a problem does not arise. In addition, a natural oxidation film is destroyed by heat treatment after gate electrode formation.
[0019] In the above, the 1st example of this invention was explained. Although this invention has covered the direct silicon nitride on a tungsten silicide film, even if the layer which consists of an another kind member in the meantime may be formed and it is wearing a part of front face of a tungsten silicide film by the silicon nitride, it is effective. Especially the latter is the problem of balance with the amount of the silicon in a tungsten silicide film, and the amount of the silicon consumed by oxidization.
[0020] Then, the 2nd example of this invention is explained. [Drawing 8] - [drawing 14] is the cross section having shown the 2nd example of this invention in order of the process. With reference to a drawing, a manufacturing process is explained in order of below.

[0021] As shown in [drawing 8], the LOCOS method is used for the isolation field on the single-crystal-silicon substrate 200 of P type, and the oxide film 201 for isolation with a thickness of 1 micrometer is formed in it. Then, the gate oxide film 202 with a thickness of 10nm is formed in the field in which the oxide film 201 for isolation on the single-crystal-silicon substrate 200 is not formed by thermal oxidation.
[0022] Then, as shown in [drawing 9], the polysilicon contest film 203 with a thickness of 100nm is formed using the LPCVD method, and Lynn which is an N type impurity is poured in using ion-implantation to the polysilicon contest film 203 concerned. Then, the insulator layer 204 between the gates of ONO structure (an oxide film, a nitride, bipolar membrane of an oxide film) is formed by oxidizing thermally on the polysilicon contest film 203 by forming the 10nm thermal oxidation film 221, continuing at this, and forming the silicon nitride 222 with a thickness of 15nm and forming the 6nm thermal oxidation film 223 on the silicon nitride concerned thermal oxidation continuously by the LPCVD method. Then, a film composition ratio (mole ratio) deposits 200nm of tungsten silicide films 205 which are W(tungsten):Si(silicon) =1:2.5-3.0 with DC magnetron-sputtering technology. Then, 100nm of 1st silicon nitride 206 is deposited using the LPCVD method.
[0023] Then, the resist which is not illustrated is formed on the 1st silicon nitride 206, and the resist pattern of 0.3-micrometer width of face is formed by using lithography technology. Etching processing is given as it is shown in [drawing 10], using this resist pattern as a mask. That is, using RIE, a gate electrode configuration is processed, the silicon nitride 206 and the tungsten silicide film 205 are combined, carrying out etching removal of the insulator layer 204 between the gates is continued, and a resist is removed. Thus, the control gate electrode was formed.
[0024] Then, the LPCVD method is used for the whole surface, the 2nd silicon nitride 207 of 100nm thickness is deposited on it, and 100nm etchback of this 2nd silicon nitride 207 is carried out using RIE technology. Consequently, as shown in [drawing 11], the 2nd silicon nitride 207 remains in the control gate electrode side-attachment-wall section.
[0025] Then, as shown in [drawing 12], RIE is given by using the 1st silicon nitride 206 and the 2nd silicon nitride 207 as a mask, and a floating gate is formed by carrying out etching processing of the polysilicon contest film 203.
[0026] Then, heat treatment called post-oxidization is usually performed. By giving such thermal oxidation, as shown in [drawing 13], the side attachment wall of the polysilicon contest film 203, i.e., a floating gate, wears a radius of circle 208, and the BAZU beak 209 is formed between a silicon substrate 200 and the polysilicon contest film 203.
[0027] Then, as shown in [drawing 14], the N type source field 210 and the N type drain field 211 are formed with an ion implantation. Then, a layer insulation film, a metal wiring (bit line) layer, etc. which are not illustrated are formed.
[0028] If the manufacturing process of the 2nd example of this invention is used as explained above, since the periphery, i.e., the upper part, and the side-attachment-wall section of a refractory-metal silicide film (control gate) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (floating gate) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.
[0029] Moreover, in the MOS transistor which has the floating gate explained in the 2nd example, the BAZU beak between a floating gate and a semiconductor substrate contributes also to improvement in a data-hold property. That is, it can prevent the charge accumulated to the floating gate emitting outside (especially drain) by the tunnel current through a gate oxide film. Moreover, it contributes also to improvement in read-out speed from a control gate electrode being a refractory-metal silicide film. following -- if the manufacturing process shown in the 2nd example is used, a nonvolatile semiconductor memory with sufficient high speed and a sufficient data-hold property can be offered
[0030] In the above, the 2nd example of this invention was explained. Although this invention has covered the direct silicon nitride on a tungsten silicide film, even if the layer which consists of an another kind member in the meantime may be formed and it is wearing a part of front face of a tungsten silicide film by the silicon nitride like the 1st example, it is effective. Especially the latter is the problem of balance with the amount of the silicon in a tungsten silicide film, and the amount of the silicon consumed by oxidization.
[0031] In addition, although the 1st and 2nd examples explained the example which uses a tungsten silicide film as a refractory-metal silicide film, it is also possible not to restrict to this and to use the refractory-metal silicide film of other types, such as a molybdenum silicide film and a titanium silicide film.
[0032]
[Effect of the Invention] If this invention is used, since the amount of oxidization of the tungsten silicide front face at the time of post-oxidization will be sharply reduced by forming a silicon nitride only on refractory-metal silicide films, such as tungsten silicide, elevation of wiring resistance can be pressed down and the reliable semiconductor device of a gate oxide film can be offered. Consequently, the product yield also improves greatly.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] this invention relates to the manufacture method of a semiconductor device. Especially, a high-melting point silicide film is used for gate polar-zone material, and it is related with the manufacture method of the ** MOS transistor which performs post-oxidation treatment for improvement in an electrical property.

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PRIOR ART

[Description of the Prior Art] Conventionally, in the manufacturing process of an MOS transistor transistor, thermal oxidation of the gate oxide film after processing of the gate electrode called post-oxidization has been performed. After this, in oxidization, the edge of a gate electrode oxidizes and it is roundish. This is called BAZU beak. The electric-field concentration in the gate edge at the time of impressing voltage to the gate is eased by this BAZU beak, and the reliability of the gate oxide film in a gate edge improves by it.
[0003] The cross section of the conventional MOS transistor is shown in [drawing 15], and the manufacture method is shown in order of a process. The LOCOS method (selective oxidation method) is used for the isolation field of P type silicon-substrate 300 front face, and the field oxide film 301 is formed in it. Then, after forming the gate oxide film 302 by thermal oxidation, the polysilicon contest film 303 is deposited and this is processed into a gate electrode configuration. Then, oxidize the polysilicon contest film 303 thermally, while forming the thermal oxidation film 304, it is made roundish at the gate electrode edge, and the BAZU beak 305 is formed between the P type silicon substrate 300 and the polysilicon contest film 303. Then, the source 306 and a drain 307 are formed by diffusing an N type impurity.
[0004] However, when forming an MOS transistor using the process which forms a BAZU beak by post-oxidization and the electric conduction film containing high-melting point silicide films, such as a tungsten silicide film, is used as gate polar-zone material, un-arranging [which is described below] arises. That is, if a thermal oxidation film is formed in a gate electrode front face after processing the gate electrode which consists of a polysilicon contest film (lower layer) and a tungsten silicide film (upper layer), the silicon of the surplus contained in tungsten silicide will be consumed, and oxidization will take place about a tungsten metal. If it oxidizes directly hereafter, without [which does not increase this] forming a natural oxidation film on a polysilicon contest film, and using side attachment walls, such as a nitride, etc. in this state, if it carries out and the bipolar membrane of a polysilicon contest film and a high-melting point silicide film will be used as a gate electrode, silicon will be prevented from moving to the upper tungsten silicide film from a lower layer polysilicon contest film. Consequently, oxidization of a tungsten silicide film will be accelerated. For this reason, the problem that wiring resistance will increase remarkably had arisen. Moreover, if thermal oxidation time is short set up in order to reduce the amount of oxidization of a tungsten silicide film, a BAZU beak will not fully be formed in a gate electrode edge, but the reliability of a gate oxide film will deteriorate.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] If this invention is used, since the amount of oxidization of the tungsten silicide front face at the time of post-oxidization will be sharply reduced by forming a silicon nitride only on refractory-metal silicide films, such as tungsten silicide, the rise of wiring resistance can be pressed down and the reliable semiconductor device of a gate oxide film can be offered. Consequently, the product yield also improves greatly.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As described above, by the manufacture method of the MOS transistor of the conventional refractory-metal silicide gate, there was a trouble that oxidization of a refractory-metal silicide film will start, consequently wiring resistance will increase by post-oxidization.
[0006] this invention aims at offering the manufacture method of the semiconductor device which forms sufficient BAZU beak collectively about a post-oxidization process, without making wiring resistance increase by removing the above-mentioned fault.

[Translation done.]

MEANS

[Means for Solving the Problem] The process which forms a policy contest film through a gate insulator layer in this invention on a semiconductor substrate in order to attain the above-mentioned purpose, The process which forms a refractory-metal silicide film on a polysilicon contest film, and the process which forms the 1st nitride on a refractory-metal silicide film, The process which etches alternatively to the 1st nitride and refractory-metal silicide film, and processes a gate electrode configuration, The process which forms the 2nd nitride in the side attachment wall of the 1st nitride and high-melting point silicide film which were processed into the gate electrode configuration, The manufacture method of the semiconductor device characterized by providing the process which etches to a polysilicon contest film by using the 1st nitride and the 2nd nitride as a mask, and the process which forms a BAZU beak between a polysilicon contest film and a semiconductor substrate by performing heat treatment is offered.

[Translation done.]

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OPERATION

[Function] If a means to provide by this invention is used, since the periphery, i.e., the upper part, and the side-attachment-wall section of a high-melting point silicide film (gate electrode upper part) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (gate electrode lower part) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.

[Translation done.]

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EXAMPLE

[Example] Each example of this invention is explained with reference to a drawing. [Drawing 1] - [drawing 7] is the cross section having shown the 1st example of this invention in order of the process. With reference to a drawing, a manufacturing process is explained in order of below.

[0010] As shown in [drawing 1], the LOCOS method (selective oxidation method) is used for the isolation field on the single-crystal-silicon substrate 100 of P type, and the oxide film 101 for isolation with a thickness of 1 micrometer is formed in it. Then, the gate oxide film 102 with a thickness of 10nm is formed in the field in which the oxide film 101 for isolation on the single-crystal-silicon substrate 100 is not formed by thermal oxidation.

[0011] Then, as shown in [drawing 2], the polysilicon contest film 103 with a thickness of 100nm is formed using the LPCVD method (reduced pressure modified chemical vapor deposition), and Lynn is introduced about [one to 5x1015cm -] two after that using ion-implantation to the polysilicon contest film 103. Then, a film composition ratio (mole ratio) deposits 200nm of tungsten silicide films 105 which are W(tungsten):Si(silicon) =1:2.5-3.0 with DC magnetron-sputtering technology. Then, 100nm of 1st silicon nitride 106 is deposited using the LPCVD method. At this time, the natural oxidation film 104 will exist between the polysilicon contest film 103 and the tungsten silicide film 105.

[0012] Then, the resist which is not illustrated is formed on the silicon nitride 106, and the resist pattern of 0.3-micrometer width of face is formed by using lithography technology. Etching processing is given as it is shown in [drawing 3], using this resist pattern as a mask. That is, the RIE (using reactive ion etching) silicon nitride 106 and the tungsten silicide film 105 are processed into a gate electrode configuration, and a resist is removed. At this time, etching removal of the natural oxidation film 104 is carried out simultaneously. Thus, the upper part of a gate electrode was formed.

[0013] Then, the LPCVD method is used for the whole surface, the 2nd silicon nitride 107 of 100nm thickness is deposited on it, and 100nm etchback of this 2nd silicon nitride 107 is carried out using RIE technology. Consequently, as shown in [drawing 4], the 2nd silicon nitride 107 remains in the gate electrode up (tungsten silicide film 105 and 1st silicon nitride 106) side-attachment-wall section.

[0014] Then, as shown in [drawing 5], RIE is given by using the 1st silicon nitride 106 and the 2nd silicon nitride 107 as a mask, and a lower gate electrode is formed by carrying out etching processing of the polysilicon contest film 103.

[0015] Then, heat treatment called post-oxidization is usually performed. By giving such thermal oxidation, as shown in [drawing 6], the side attachment wall of the polysilicon contest film 103 wears a radius of circle 108, and the BAZU beak 109 is formed between a silicon substrate 100 and the polysilicon contest film 103.

[0016] Then, as shown in [drawing 7], the N type source field 110 and the N type drain field 111 are formed with an ion implantation. Then, a layer insulation film, a metal wiring layer, etc. which are not illustrated are formed.

[0017] If the manufacturing process of this invention is used as explained above, since the periphery, i.e., the upper part, and the side-attachment-wall section of a high-melting point silicide film (gate electrode upper part) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (gate electrode lower part) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.

[0018] In addition, usually, if the bipolar membrane of a polysilicon contest film and a high-melting point silicide film is used as a gate electrode, a natural oxidation film will be formed on a polysilicon contest film. In this state, after oxidizing directly, without using side attachment walls, such as a nitride, etc., silicon was prevented from moving to the upper tungsten silicide film from the polysilicon contest film of a lower layer [film / natural oxidation], and oxidization of the tungsten silicide film concerned was accelerated. However, in this example, even if a natural oxidation film is formed and movement of silicon is oppressed, since the up gate electrode is covered by the nitride, a problem does not arise. In addition, a natural oxidation film is destroyed by heat treatment after gate electrode formation.

[0019] In the above, the 1st example of this invention was explained. Although this invention has covered the direct silicon nitride on a tungsten silicide film, even if the layer which consists of an another kind member in the meantime may be formed and it is wearing a part of front face of a tungsten silicide film by the silicon nitride, it is effective. Especially the latter is the problem of balance with the amount of the silicon in a tungsten silicide film, and the amount of the silicon consumed by oxidization.

[0020] Then, the 2nd example of this invention is explained. [Drawing 8] - [drawing 14] is the cross section having shown the 2nd example of this invention in order of the process. With reference to a drawing, a manufacturing process is explained in order of below.
[0021] As shown in [drawing 8], the LOCOS method is used for the isolation field on the single-crystal-silicon substrate 200 of P type, and the oxide film 201 for isolation with a thickness of 1 micrometer is formed in it. Then, the gate oxide film 202 with a thickness of 10nm is formed in the field in which the oxide film 201 for isolation on the single-crystal-silicon substrate 200 is not formed by thermal oxidation.
[0022] Then, as shown in [drawing 9], the polysilicon contest film 203 with a thickness of 100nm is formed using the LPCVD method, and Lynn which is an N type impurity is poured in using ion-implantation to the polysilicon contest film 203 concerned. Then, the insulator layer 204 between the gates of ONO structure (an oxide film, a nitride, bipolar membrane of an oxide film) is formed by oxidizing thermally on the polysilicon contest film 203 by forming the 10nm thermal oxidation film 221, continuing at this, and forming the silicon nitride 222 with a thickness of 15nm and forming the 6nm thermal oxidation film 223 on the silicon nitride concerned thermal oxidation continuously by the LPCVD method. Then, a film composition ratio (mole ratio) deposits 200nm of tungsten silicide films 205 which are W(tungsten):Si(silicon) =1:2.5-3.0 with DC magnetron-sputtering technology. Then, 100nm of 1st silicon nitride 206 is deposited using the LPCVD method.
[0023] Then, the resist which is not illustrated is formed on the 1st silicon nitride 206, and the resist pattern of 0.3-micrometer width of face is formed by using lithography technology. Etching processing is given as it is shown in [drawing 10], using this resist pattern as a mask. That is, using RIE, a gate electrode configuration is processed, the silicon nitride 206 and the tungsten silicide film 205 are combined, carrying out etching removal of the insulator layer 204 between the gates is continued, and a resist is removed. Thus, the control gate electrode was formed.
[0024] Then, the LPCVD method is used for the whole surface, the 2nd silicon nitride 207 of 100nm thickness is deposited on it, and 100nm etchback of this 2nd silicon nitride 207 is carried out using RIE technology. Consequently, as shown in [drawing 11], the 2nd silicon nitride 207 remains in the control gate electrode side-attachment-wall section.
[0025] Then, as shown in [drawing 12], RIE is given by using the 1st silicon nitride 206 and the 2nd silicon nitride 207 as a mask, and a floating gate is formed by carrying out etching processing of the polysilicon contest film 203.
[0026] Then, heat treatment called post-oxidization is usually performed. By giving such thermal oxidation, as shown in [drawing 13], the side attachment wall of the polysilicon contest film 203, i.e., a floating gate, wears a radius of circle 208, and the BAZU beak 209 is formed between a silicon substrate 200 and the polysilicon contest film 203.
[0027] Then, as shown in [drawing 14], the N type source field 210 and the N type drain field 211 are formed with an ion implantation. Then, a layer insulation film, a metal wiring (bit line) layer, etc. which are not illustrated are formed.
[0028] If the manufacturing process of the 2nd example of this invention is used as explained above, since the periphery, i.e., the upper part, and the side-attachment-wall section of a refractory-metal silicide film (control gate) are surrounded by the 1st nitride and the 2nd nitride, in the post-oxidization process after processing a gate configuration, oxidization of the high-melting point silicide film concerned will be suppressed. However, since the flank of a polysilicon contest film (floating gate) is not covered by the nitride, a post-oxidization process oxidizes thermally and a BAZU beak is formed between semiconductor substrates. Consequently, the reliability of a gate insulator layer can be improved, without reducing resistance of a gate electrode.
[0029] Moreover, in the MOS transistor which has the floating gate explained in the 2nd example, the BAZU beak between a floating gate and a semiconductor substrate contributes also to improvement in a data-hold property. That is, it can prevent the charge accumulated to the floating gate emitting outside (especially drain) by the tunnel current through a gate oxide film. Moreover, it contributes also to improvement in read-out speed from a control gate electrode being a refractory-metal silicide film. following -- if the manufacturing process shown in the 2nd example is used, a nonvolatile semiconductor memory with sufficient high speed and a sufficient data-hold property can be offered
[0030] In the above, the 2nd example of this invention was explained. Although this invention has covered the direct silicon nitride on a tungsten silicide film, even if the layer which consists of an another kind member in the meantime may be formed and it is wearing a part of front face of a tungsten silicide film by the silicon nitride like the 1st example, it is effective. Especially the latter is the problem of balance with the amount of the silicon in a tungsten silicide film, and the amount of the silicon consumed by oxidization.
[0031] In addition, although the 1st and 2nd examples explained the example which uses a tungsten silicide film as a refractory-metal silicide film, it is also possible not to restrict to this and to use the refractory-metal silicide film of other types, such as a molybdenum silicide film and a titanium silicide film.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

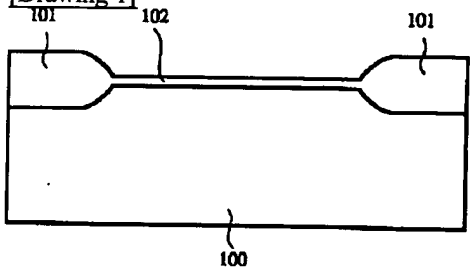
[Brief Description of the Drawings]
[Drawing 1] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 2] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 3] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 4] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 5] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 6] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 7] The cross section having shown the 1st example of this invention in order of the process.
[Drawing 8] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 9] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 10] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 11] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 12] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 13] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 14] The cross section having shown the 2nd example of this invention in order of the process.
[Drawing 15] The cross section having shown the conventional semiconductor device.
[Description of Notations]
100 Silicon Substrate
101 Insulator Layer for Isolation
103 Polysilicon Contest Film
104 Natural Oxidation Film
105 Tungsten Silicide Film
106 Silicon Nitride
107 Silicon Nitride
108 Radius of Circle of Polysilicon Contest Film Side Attachment Wall
109 BAZU Beak
110 Source
111 Drain

[Translation done.]

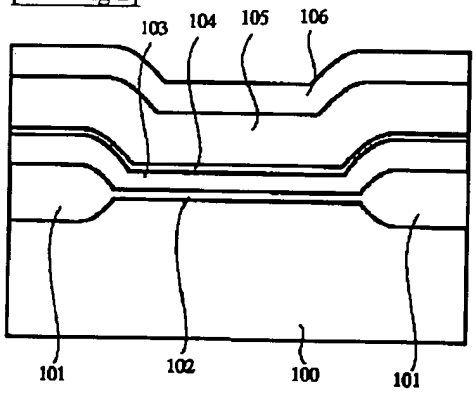
* NOTICES *

DRAWINGS

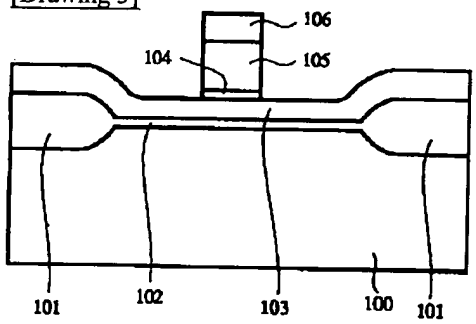
[Drawing 1]



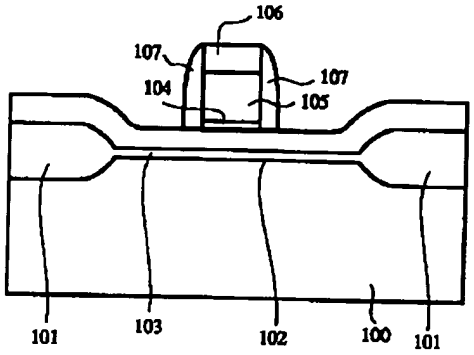
[Drawing 2]



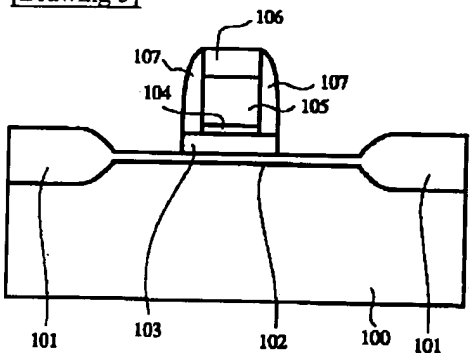
[Drawing 3]



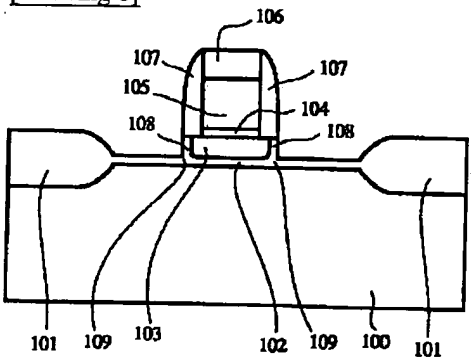
[Drawing 4]



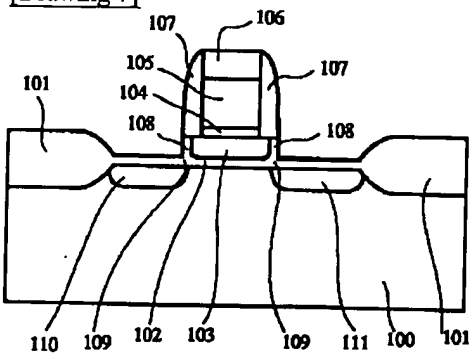
[Drawing 5]



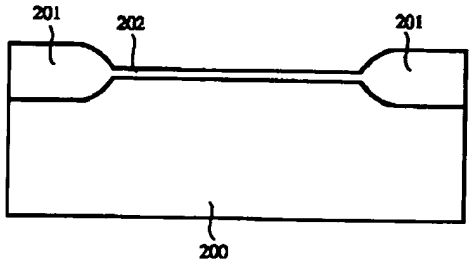
[Drawing 6]



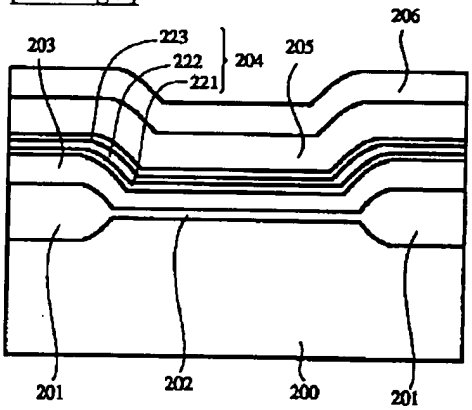
[Drawing 7]



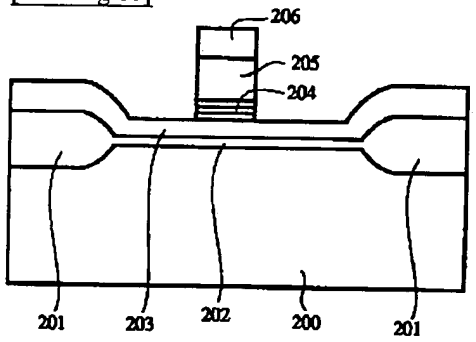
[Drawing 8]



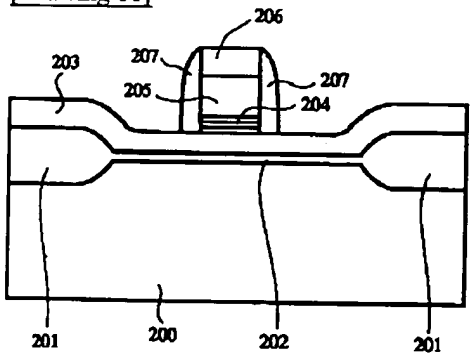
[Drawing 9]



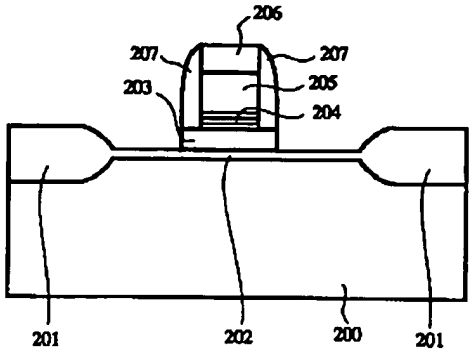
[Drawing 10]



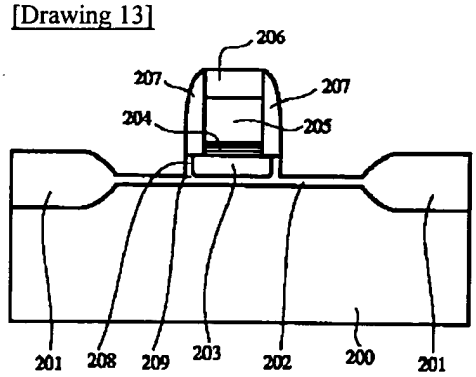
[Drawing 11]



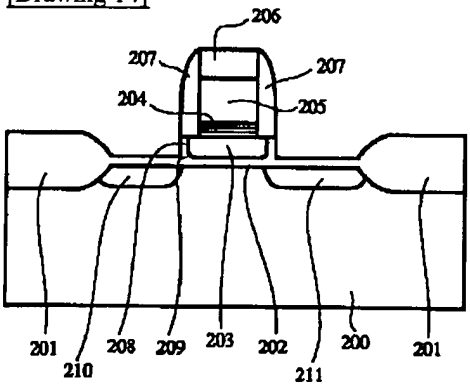
[Drawing 12]



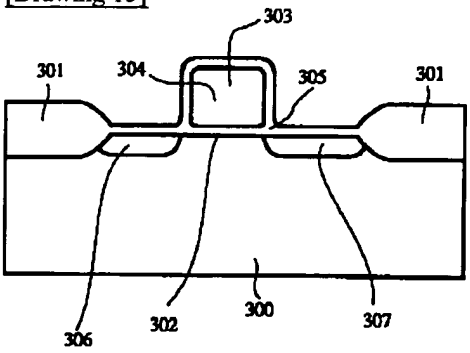
[Drawing 13]



[Drawing 14]



[Drawing 15]



[Translation done.]